# DIPLEXER DESIGN: Q-MATCHING TECHNIQUES

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## Abstract

Many radio stations are considering diplexed systems because the costs of constructing a new site are higher than the cost of diplexing. Diplexing eliminates the need and cost of a separate tower, ground system, transmitter building, and site. To take advantage of the cost savings, a diplexer is required.

The Q-Matching technique is a method for choosing the value of each component to provide a diplex system with optimized bandwidth characteristics. It is the purpose of this paper to demonstrate the Q- Matching optimization technique that will minimize the effect the traps have on the bandwidth of both stations. At the same time, this technique will generally increase the isolation between the two stations over other designs.

## Introduction

A diplexer is a set of traps that will allow the operation of two frequencies on the same antenna. Figure 1 shows a schematic representation of a diplexer. Although all parts are not necessary in every case, there are basically 5 parts to a diplexer.

The Antenna Coupling Unit (ACU) is used to match the impedance of the antenna to the $Z_o$ of the transmission line. There are two ACUs; one for each frequency. Their design will not be discussed.

The Auxiliary Trap is used to further attenuate the reject frequency. It provides a high impedance to ground at the pass frequency (on the order of 10K ohms) and a low impedance to ground at the reject frequency (on the order of 1 ohm). There is one Auxiliary trap for each frequency.

The Antenna Resonator is a coil if the impedance at that point is capacitive, and a capacitor if the impedance is inductive. It is used to bring the impedance to the point where the Auxiliary Trap will be connected to the circuit close to resonance. This near resonance condition is necessary when employing the Q-Matching technique. There may be one antenna resonator for each frequency.

The Main Trap is used to attenuate the reject frequency. It provides a high impedance at the reject frequency (on the order of 10K ohms) and a low impedance at the pass frequency (on the order of 1 ohm). There are two Main Traps in a diplexer, one for each frequency.

The Diplex Point is where the two signals first come together. The impedances at this point are what is used in the calculations of

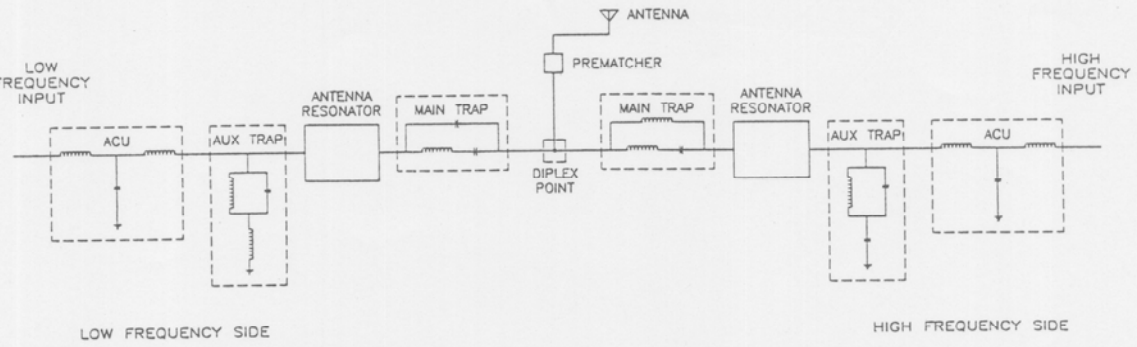



Figure 1 - Diplexer Schematic

stresses and Qs, for the trap circuitries. It is desirable to have the branch point impedance at each frequency to be close to resonance. Also, it is desirable for the parallel resistance to be somewhere between 50 and 200 ohms. Each Main Trap stores energy at the pass and the reject frequency. These criteria will provide enough series resistance so the Main Trap's Q will not be too high at the pass frequency. Also, a parallel resistance of 50 to 200 ohms is not too high so the Main Trap's Q will not be too high at the reject frequency. To aid in providing an improved impedance at the diplex point, a prematcher may be used. It consists of a combination of coils and capacitors which will make the diplex point impedances better at both frequencies. There is no set way for designing a prematcher, but an example will be given later in the paper to demonstrate its purpose.

## Filter Classes

There are four different types of notch filters or traps that are generally used in the design of diplexers: two Main Trap types and two Auxiliary Trap types.

Figure 2 shows the two types of Main Traps. The first, which will be referred to as the Series Main Trap, consists of a coil and capacitor in series resonance at the pass frequency. Also, a third component is placed in parallel with the series combination of the first two. The third component is in parallel resonance with the series combination of the first two components C1 and L1 at the reject frequency. The third component is a capacitor if the reject frequency is higher than the pass frequency and is a coil if the reject frequency is lower than the pass frequency.

of the first two. The third component is in series resonance with the parallel combination of the first two components C1 and L1 at the pass frequency. The third component is a capacitor if the reject frequency is higher than the pass frequency, and is a coil if the reject frequency is lower than the pass frequency.

Figure 3 shows the two types of Auxiliary Traps. The first, which will be referred to as the Series Auxiliary Trap, consists of a coil and capacitor in series resonances to ground at the reject frequency. A third component is placed in parallel with the series combination of the first two. The third component is in parallel resonance with the series combination of the first two components C1 and L1 at the pass frequency. The third component is a capacitor if the pass frequency is higher than the reject frequency, and is a coil if the pass frequency is lower than the reject frequency.

The second Auxiliary Trap type which will be referred to as the Parallel Auxiliary Trap, consists of a coil and capacitor in parallel resonances at the pass frequency. A third component is placed in series to ground with the parallel combination of the first two. The third component is in series resonance with the parallel combination of the first two components C1 and L1 at the reject frequency. The third component is a capacitor if the pass frequency is higher than the reject frequency, and is a coil if the pass frequency is lower than the reject frequency.

## Component Values

In this section the equations for the component values of each type of trap will be given. Each trap component is defined when the

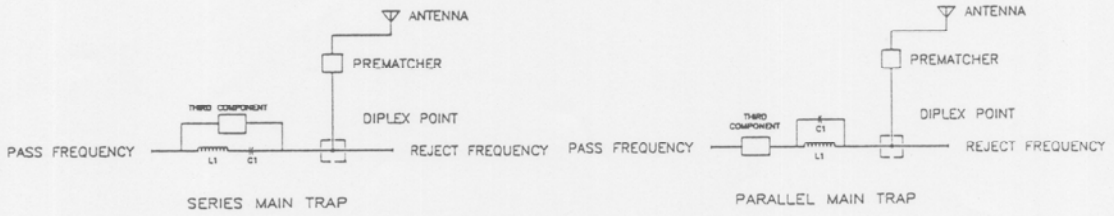



Figure 2 - Main Trap Types

The second Main Trap class which will be referred to as the Parallel Main Trap, consists of a coil and capacitor in parallel resonances at the reject frequency. A third component is placed in series with the parallel combination

component C1 is chosen and the frequencies are known. In the equations below, $W_L$ will be the radian frequency of the lower frequency. $W_H$ will be the radian frequency of the higher frequency. F will be the ratio of the low frequency to the high frequency.

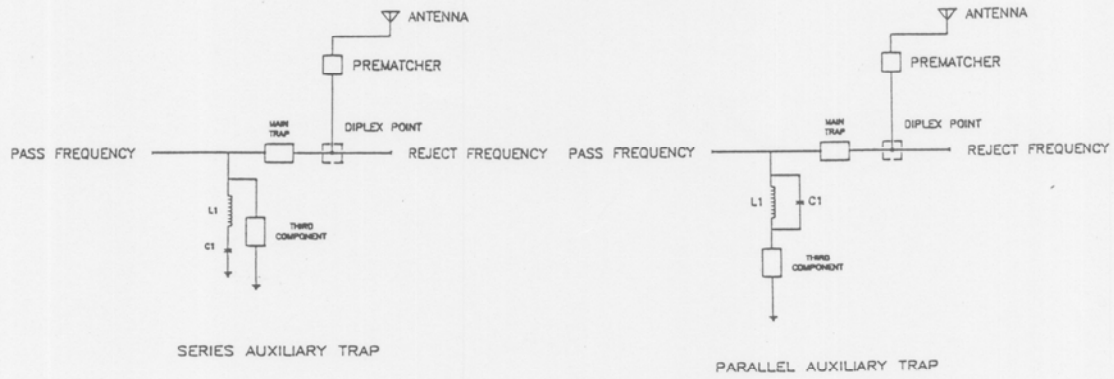



Figure 3 - Auxiliary Trap Types

$W_L = 2 \times PI \times F_L$ where $F_L$ is the low frequency

$W_H = 2 \times PI \times F_H$ where $F_H$ is the high frequency

$F = F_L / F_H$ F is the frequency ratio

Refer to Figures 4-7 on pages 4 and 5 for a schematic drawing. The equations for the components of each type of trap are given below.

Series Main Trap Low Frequency Side

$$L1 = 1/ (W_L^2 \times C1)$$

$$C2 = (C1 \times F^2) / 1 - F^2$$

Series Main Trap High Frequency Side

$$L1 = 1 / (W_H^2 \times C1)$$

$$L2 = (1 - F^2) / (W_L^2 \times C1)$$

Parallel Main Trap Low Frequency Side

$$L1 = 1 / (W_H^2 \times C1)$$

$$C2 = C1 \times (1 - F^2) / F^2$$

Parallel Main Trap High Frequency Side

$$L1 = 1 / (W_L^2 \times C1)$$

$$L2 = 1 / [(W_H^2 - W_L^2) \times C1]$$

Series Auxiliary Trap Low Frequency Side

$$L1 = 1 / (W_H^2 \times C1)$$

$$L2 = (1 - F^2) / (W_L^2 \times C1)$$

Series Auxiliary Trap High Frequency Side

$$L1 = 1 / (W_L^2 \times C1)$$

$$C2 = (C1 \times F^2) / (1 - F^2)$$

Parallel Auxiliary Trap Low Frequency Side

$$L1 = 1 / (W_L^2 \times C1)$$

$$L2 = 1 / [(W_H^2 - W_L^2) \times C1]$$

Parallel Auxiliary Trap High Frequency Side

$$L1 = 1 / (W_H^2 \times C1)$$

$$C2 = C1 \times (1 - F^2) / F^2$$

Bandwidth of Diplex System

It will be shown that different choices for the component C1 will affect the Loaded Q of the trap at both frequencies, thus the bandwidth of the system. Loaded Q is defined in the usual way. The equation for the Loaded Q is given below.

$$\text{Loaded Q} = (2 \times PI \times MSE) / DE$$

where MSE is the maximum stored energy and DE is the energy dissipated per cycle.

Consider the Loaded Qs for a Parallel Main Trap on the high frequency side. The Loaded Qs are as follows.

$$Q_L = RP_L \times W_L \times C1$$

$$Q_H = (W_H \times L2 \times Q_M) / R_H$$

where $RP_L$ is the parallel resistance of the diplex point at the low frequency, $R_H$ is the series resistance of the diplex point at the high frequency, and $Q_M$ is the Q multiplier.

If a substitution for L2 is made, the second equation becomes as follows.

$$Q_H = (W_H \times Q_M) / [R_H \times C1 \times (W_L^2 - W_H^2)]$$

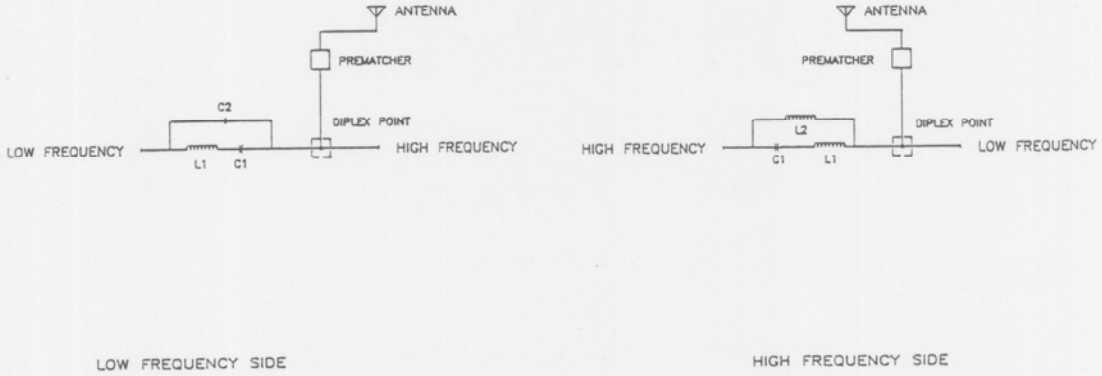



Figure 4 - Series Main Trap

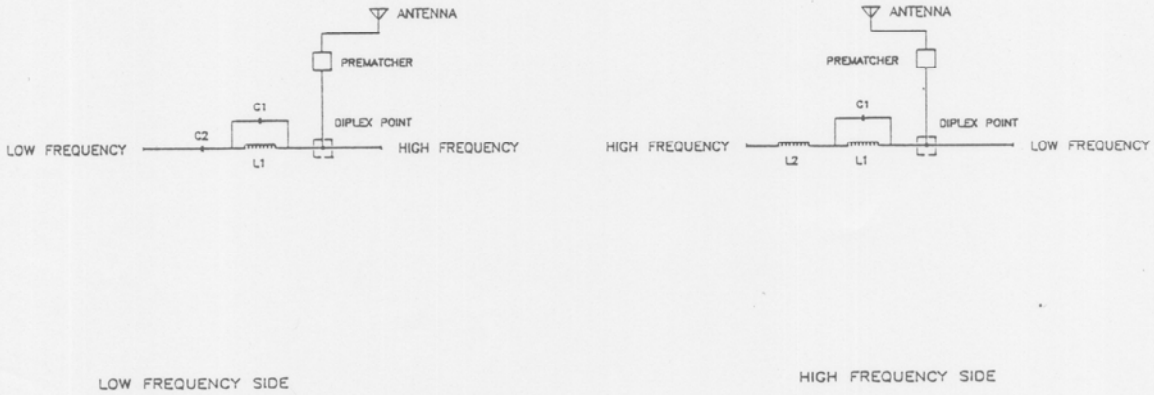



Figure 5 - Parallel Main Trap

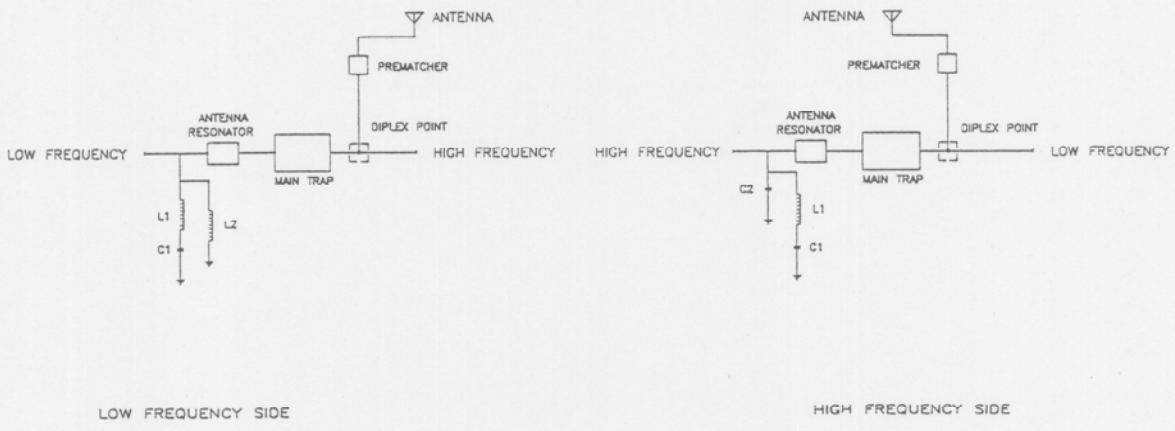
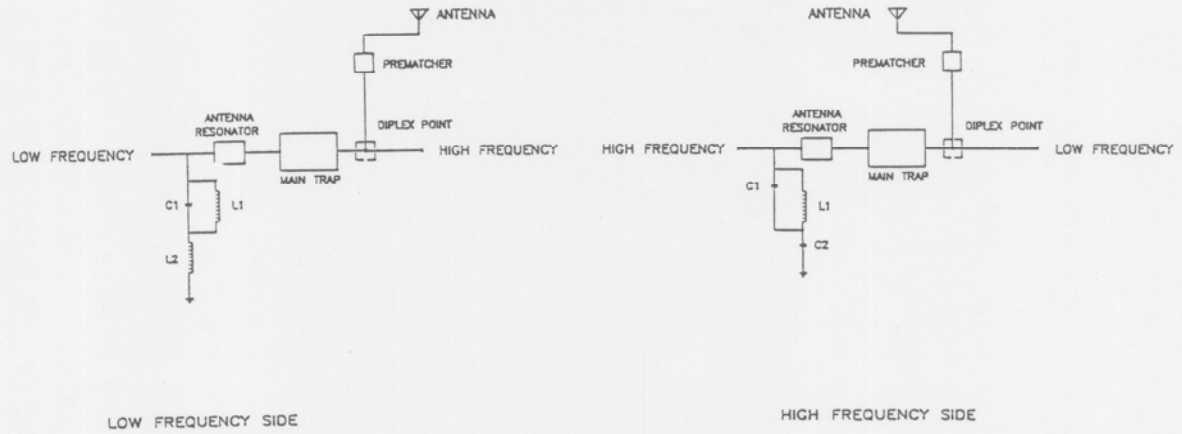



Figure 6 - Series Auxiliary Trap




LOW FREQUENCY SIDE

HIGH FREQUENCY SIDE

Figure 7 - Parallel Auxiliary Trap

Note that C1 is in the numerator for the equation for $Q_L$ but in the denominator for the equation for $Q_H$. This means that as C1 gets smaller, $Q_L$ gets smaller, and $Q_H$ gets larger. Also as C1 gets larger, $Q_L$ gets larger, and $Q_H$ gets smaller. Therefore, in this case, if C1 is chosen to be relatively small, the stored energy in the high frequency system would increase, thus negatively affecting the bandwidth. Also if C1 is chosen to be relatively large, the bandwidth of the low frequency would be adversely affected.

One solution to the problem would be to choose a capacitor such that the Loaded Q for each frequency is the Same. This could be done by setting $Q_L$ equal to $Q_H$ and solving for C1. For this case, $C1^2$ would be as follows.

$$C1^2 = (W_H \times Q_M) / [RP_L \times W_L \times R_H \times (W_H^2 - W_L^2)]$$

This design method for choosing C1 will be referred to later as the standard design. When the Q-Matching technique is discussed, it will be shown that this is not the best solution for C1.

Unloaded Q and Rejection

To estimate the isolation that a Main Trap will produce, it is necessary to calculate its parallel resistance at the reject frequency. This parallel resistance will be called the reject resistance (using the symbol RR) to avoid the confusion with the parallel resistance of the diplex point. The magnitude of this reject resistance is generally on the order of 10 K ohms. The reject resistance is a function of the Unloaded Q ($Q_U$) of the coil. The Unloaded Q is the ratio of the reactance of the coil and its resistance. Unloaded Qs of coils used for diplexers are typically between 200 and 800.

To estimate the isolation that an Auxiliary Trap will produce, it is necessary to calculate its series resistance (RS) to ground at the reject frequency. The magnitude of the series resistance is on the order of 1 ohm. The series resistance is also a function of the Unloaded Q of the coils used in the trap.

Loaded Q and Rejection

The isolation that a trap will produce is also a function of the Loaded Q of the trap at the pass frequency. It was shown earlier that the Loaded Q of a Parallel Main Trap on the high frequency side could be expressed with the following equation.

$$Q_H = (W_H \times Q_M) / [R_H \times C1 \times (W_H^2 - W_L^2)]$$

The reject resistance of this trap is $W_L \times L1 \times Q_U$. If a substitution is made for L1, the reject resistance for a parallel trap on the high frequency side would be as follows.

$$RR_H = Q_U / (W_L \times C1)$$

It can be seen by inspection that if C1 is small, the Loaded Q of the trap and its reject resistance are high. This means that the higher the Loaded Q of the trap, the better the rejection of the trap.

$Q_U$ is not constant for all coils. As the inductance of a coil increases, its $Q_U$ will generally increase. For the above example, the reject resistance would increase faster than 1/C1 as C1 gets smaller.

## Q-Matching Techniques

In the previous sections it was shown that the Loaded Q of a Main Trap affects the bandwidth of the system and its rejection resistance. In this section the Q-Matching technique will be discussed. To assist in the understanding of the Q-Matching technique, several circuits will be analyzed.

Consider the circuit in Figure 8. The circuit has a Loaded Q of 4 and produces a 1.083:1 VSWR at the 10 kHz sideband frequencies. Compare this to the circuit in Figure 9. This circuit has a Loaded Q of 8 but produces a VSWR at the 10 kHz sideband frequencies of only 1.006:1. The circuit in Figure 9 contains two parts. The first part is a series network with a Loaded Q of 4. The second part is a parallel circuit with a Loaded Q of 4. This circuit, which has a Loaded Q of 8, is producing VSWRs of the same magnitude as a series circuit with a Loaded Q of .32.

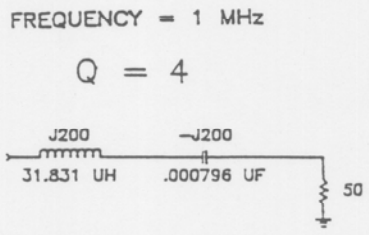



Figure 8
VSWR at the 10 kHz Sideband
Frequencies is 1.083:1

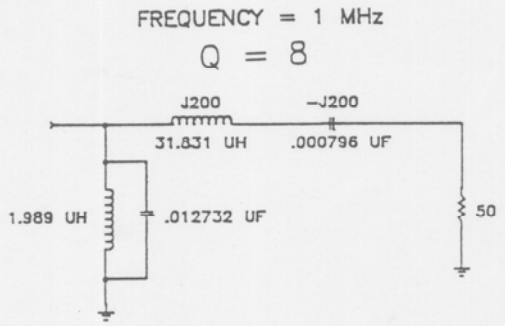



Figure 9
VSWR at the 10 kHz Sideband
Frequencies is 1.006:1

Equivalent Q ($Q_E$) of a circuit or system will be defined as the Loaded Q of a series resonant circuit which produces the same VSWRs at the 10 kHz sideband frequencies as the original circuit. The equation for equivalent Q is given below.

$$Q_E = (F_c / .02) \times [SQRT(VSWR) - 1 / SQRT(VSWR)]$$

Where $F_c$ is the carrier frequency in MHz.

The circuit in Figure 9 would have a $Q_E$ of .32 and a Loaded Q of 8. By making the Loaded Q of the series part of the circuit equal to the Loaded Q of the parallel part of the circuit, the $Q_E$ of the circuit is much lower than the Loaded Q. This technique of reducing the $Q_E$ of a circuit in this manner will be referred to as Q-Matching.

Table 1 below shows the degree to which the $Q_E$ of a series resonant circuit could be reduced by adding an additional parallel circuit of the same Loaded Q. This table is for 1 MHz. To adjust this table for different frequencies, multiply each column by the new frequency in MHz. For example, a circuit with a Q of 10 could be reduced to a $Q_E$ of 1.96 at 1 MHz. At .5 MHz a circuit with a Q of 10 (20 x .5) could only be reduced to 3.72 (7.43 x .5).

TABLE 1

| Loaded Q of Series Circuit | $Q_E$ of Series and Parallel Circuit |
|---|---|
| 2 | .08 |
| 4 | .32 |
| 6 | .71 |
| 8 | 1.26 |
| 10 | 1.93 |
| 15 | 4.31 |
| 20 | 7.43 |
| 25 | 11.18 |
| 30 | 15.43 |
| 35 | 20.07 |
| 40 | 24.99 |
| 50 | 35.36 |

It can be seen from Table 1 that the $Q_E$s of circuits that have a lower Loaded Q are reduced proportionally more than the circuits with higher Loaded Qs. Where the ratio of Q to $Q_E$ for a network with a Loaded Q of 2 is 25:1, the Q to $Q_E$ ratio of a network with a Loaded Q of 10 is only 5:1.

To obtain these reductions in $Q_E$, the point at which the parallel circuit attaches must be a purely resistive load. Using a network with a Loaded Q of the series part is 10 and a load impedance of 50 + j 50 ohms instead of 50 ohms, the $Q_E$ of the circuit calculates to be 22. This is much higher than the $Q_E$ of 1.96 which was calculated with the circuit looking into a purely resistive load.

This same principle can be used in the design of a diplexer. A Main Trap of a diplexer could be looked at as a resonant circuit in series with a load. The Auxiliary Trap is a parallel resonant circuit shunt to the load. Consider the following example:

| Station Number | Frequency (MHz) | Diplex Point Resistance (ohms) | Impedance Reactance (ohms) |
|---|---|---|---|
| 1 | 1.0 | 50 | 70 |
| 2 | 1.2 | 200 | -100 |

Table 2 contains the loaded Qs of a Parallel Main Trap on the low frequency side of the diplexer for several values of C1.

TABLE 2

| C1 (uf) | $Q_L$ | $Q_H$ |
|---|---|---|
| .001 | 23.7 | 1.9 |
| .0015 | 15.8 | 2.8 |
| .002 | 11.8 | 3.8 |
| .003 | 7.9 | 5.7 |
| .0035 | 6.8 | 6.6 |
| .004 | 5.9 | 7.5 |
| .005 | 4.7 | 9.4 |

As suggested earlier, one choice for C1 might be .0035 uf. This value gives about the same Loaded Qs for each frequency. For this case it is expected that the $Q_E$ of the load as seen by each transmitter would increase by about 6.7 due to this trap alone. Add to this the effects of the Main Trap on the high frequency side, and the Auxiliary Traps on both sides. The total system bandwidth would be greatly reduced.

Very little can be done to reduce the $Q_H$ of this network. But, the $Q_L$ in Table 2 could be reduced to a much lower $Q_E$ by using the Auxiliary Trap to Q-Match the Main Trap. To apply this technique, an Auxiliary Trap is chosen that has the same Loaded Q as the Main Trap. Also, it is necessary for the impedance at which the Auxiliary Trap is to be attached to be close to resonance. Table 3 would result if Table 2 is redone assuming the Main Trap is to be Q-Matched with the Auxiliary Trap.

TABLE 3

| C1 (uf) | $Q_E$ (Q-Matched) | $Q_H$ |
|---|---|---|
| .001 | 10.1 | 1.9 |
| .0015 | 4.8 | 2.8 |
| .002 | 2.7 | 3.8 |
| .003 | 1.2 | 5.7 |
| .0035 | 0.9 | 6.6 |
| .004 | 0.7 | 7.5 |
| .005 | 0.5 | 9.4 |

Using Table 3 above, a better choice for C1 would be a .002 uf capacitor. The $Q_E$s of Table 3 contain the effects of both the Main and Auxiliary Trap on the low frequency side. The Qs in Table 2 show only the effect of the Main Trap.

Employing the Q-Matching technique, the trap would have a higher Q. The reject resistance for this trap would then be larger. Assuming an Unloaded Q of the coils in this example to be 500, the reject resistance for the trap choosing C1 as a .0035 uf capacitor would be 19 K ohms. If C1 is a .002 uf capacitor, the reject resistance would be 33 K ohms. By choosing the .002 uf capacitor over the .0035 uf capacitor, the isolation from the high to low frequency port would be improved.

By employing the Q-Matching technique, not only will the impedance bandwidth of the system be improved over other designs, but the isolation will also be improved.

## Prematching Circuits

As mentioned earlier, there is no set way to design a prematching circuit. The purpose of a prematching circuit is to bring the tower resistance between 50 ohms and 200 ohms and keep the reactance near zero for both frequencies at the same time. This is rarely possible.

Consider an example where the frequencies of operation are 1 MHz and 1.2 MHz. Let the tower height be 300 feet tall. At 1 MHz the electrical height would be about 110 degrees. At 1.2 MHz the tower height would be about 130 degrees. These tower heights have impedances of about 135 + j 210 ohms and 420 + j 310 ohms. Let these impedances be used for the diplex point impedances. Assume that C1 is chosen for the Main Traps so that the Qs at the low and high frequencies are the same. Then the Qs for the Main Traps on the low and high frequency sides would be 6.6 and 3.1 respectively.

By inserting a capacitor of .00075 uf in series with the tower, the new diplex point impedances for the low and high frequencies would be 135 - j 2 ohms and 420 + j 133 ohms. Although the series resistance was not changed by this prematching network, the parallel resistance was lowered. For 1 MHz the parallel resistance went from 462 ohms to 135 ohms. For 1.2 MHz the parallel resistance went from 649 ohms to 462 ohms. Because the parallel resistances of the diplex point were reduced and the series resistance was unchanged, the bandwidth of the diplexer can be expected to be improved over a system which does not include a prematching network. Again assume that C1 is chosen so that the Qs at the low and high frequencies are the same. Then the Qs for the Main Traps on the low and high frequency sides for these diplex point impedances would be 5.5 and 1.7 respectively. Thus the bandwidth potential for the diplexed system would be increased with the capacitor placed in series with the tower.

## Example

In this section the results of analyses will be shown for two diplex systems. One system will be designed using the standard design technique discussed at the end of the Bandwidth of Diplex System section. The second system will employ the Q-Matching technique for diplexer design. For simplicity, all unloaded Qs for the analyses are assumed to be 500.

The design paramaters for the sample problem are given below.

| Frequency (kHz) | Tower Height (Degrees) | Impedance (ohms) | $Q_Z$ |
|---|---|---|---|
| 1000 | 90 | 55 + j 60 | 5.4 |
| 1100 | 99 | 82 + j 116 | 4.6 |

Figures 10 and 11 show the results of the bandwidth analysis done at the low and high frequencies respectively. For the low frequency, the standard design system had an equivalent Q of 8.2 compared to the equivalent Q of the Q-Matched system of 6.6. Both of these numbers can be compared to the equivalent Q of the antenna itself of 5.4. The equivalent Q of 5.4 is what could be expected if the system was not diplexed.

EQUIVALENT Q

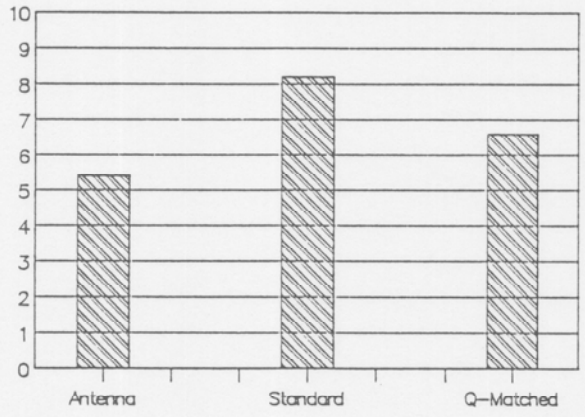



Figure 10 - Low Frequency

EQUIVALENT Q

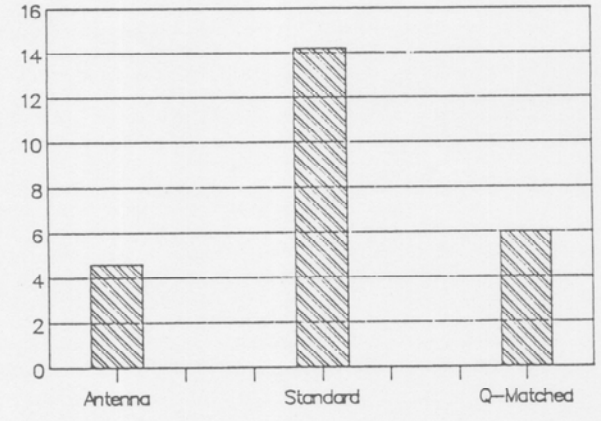



Figure 11 - High Frequency

For the high frequency, the standard design system had an equivalent Q of 14.2 compared to the equivalent Q of 6.0 for the Q-Matched system. Both of these numbers can be compared to the equivalent Q of the antenna itself of 4.6.

Figure 12 compares the port to port isolation of the two diplexer designs. The low to high frequency isolation for the standard design is 66 dB. For the Q-Matched system the port to port isolation is 88 dB. This is over a 20 dB increase in isolation.

PORT TO PORT ISOLATION

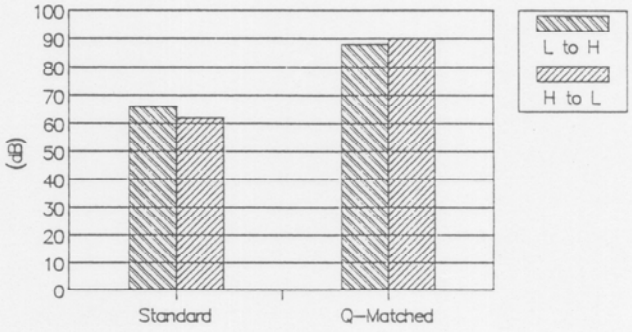



Figure 12

The high to low frequency isolation for the standard design is 62 dB. For the Q-Matched system the port to port isolation is 90 dB. This is nearly a 30 dB increase in isolation.

## Conclusion

In this paper, equations are given that are relevant to the design of diplexers for AM radio stations. In the section titled Component Values, the equations for each of the four trap types are expressed as a function of C1. These equations can be used to design the most common traps used in diplexed systems.

It was shown that the bandwidth of a diplex system is affected by the choice of filter components used in the design. By the use of the Q-Matching technique the negative effect of the diplexer on the bandwidth of the system can be minimized. Figures 10 and 11 show the improvement in $Q_E$ at the low and high frequencies by employing the Q-Matching technique.

Also, by using the Q-Matching technique, the port to port isolation will be improved. For the sample problem presented, the port to port isolation was increased by more than 20 dB.